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HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,564	HOOKER, RODNEY E.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/04, 12/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *12/14/05, 1/23/06*.

DETAILED ACTION

Claim Objections

1. Claim 24 is objected to because of the following informalities: On line 2, Examiner believes "based a determination" is a grammatical error and should be replaced with "based on a determination".

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 18-19 and 38 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

3. Claim 18 recites a computer data signal embodied in a transmission medium comprising computer-readable program code that provides the cache memory. Computer-readable program code embodied in an electronic signal or carrier wave rather than a tangible computer storage medium such as a magnetic disk or optical disk is software per se, and is non-statutory. Applicant's definition of transmission medium includes non-statutory subject matter such as carrier waves (par. 247).

4. Claim 19 recites a computer program product comprising a computer usable medium having computer readable program code that provides the cache memory. Computer readable program code embodied in an electronic signal or carrier wave rather than a tangible computer storage medium such as a magnetic disk or optical disk

is software per se, and is non-statutory. Applicant's definition of computer usable medium includes transmission mediums, which include non-statutory subject matter such as carrier waves (par. 247).

5. Claim 38 recites a computer data signal embodied in a transmission medium comprising computer-readable program code. Computer-readable program code embodied in an electronic signal or carrier wave rather than a tangible computer storage medium such as a magnetic disk or optical disk is software per se, and is non-statutory. Applicant's definition of transmission medium includes non-statutory subject matter such as carrier waves (par. 247).

Claim Rejections - 35 USC § 112

6. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear from the claim what functions that the computer readable program code causes the cache memory to perform.

Claim Rejections - 35 USC § 102

7. Claims 1-6, 8, 15-21, 23, 26-35 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Mathews, US Patent 5,956,752.

8. With respect to claim 1, Mathews teaches a cache memory comprising:

a plurality of storage elements, arranged as a last-in-first-out memory, having a top one of said plurality of storage elements for storing a cache line of data specified by

a plurality of most recent push instructions, and for storing a virtual address of said cache line, in fig. 5, memory array 160. In one embodiment of Mathews invention, this memory can act as a LIFO. See col. 5, lines 20-27, where it is disclosed that stack push and pop operations can be performed. It is also apparent from the specification that this memory array stores both a virtual address and physical address, as the memory array can be accessed by both virtual and physical address;

a comparator, coupled to said top storage element, for comparing said cache line virtual address with a source virtual address of data requested by a load instruction, in fig. 5, comparator 140 and described in col. 5, lines 28-30; and

an output, coupled to said comparator, for indicating said data requested by said load instruction is present in the cache memory if said comparator indicates said source virtual address matches said cache line virtual address stored in said top storage element, prior to determining whether a source physical address of said data requested by said load instruction matches said physical line address, in fig. 5, prediction wrong signal 178. See the related discussion in col. 5, lines 28-36.

9. With respect to claim 2, Mathews teaches the cache memory of claim 1, wherein said source physical address and said physical cache line address each comprise an upper portion of translated address bits and a lower portion of untranslated address bits, in fig. 3 and described in col. 4, lines 4-14.

10. With respect to claim 3, Mathews teaches the cache memory of claim 2, wherein said translated address bits comprise an address of a physical memory page, wherein

said untranslated address bits comprise an offset within said physical memory page, in fig. 3 and described in col. 4, lines 4-14.

11. With respect to claim 4, Mathews teaches the cache memory of claim 2, wherein said source virtual address comprises said untranslated address lower portion of said source physical address, in fig. 3 and described in col. 4, lines 4-14.

12. With respect to claim 5, Mathews teaches the cache memory of claim 4, wherein said source virtual address further comprises an upper portion of untranslated address bits appended to said untranslated lower portion, in fig. 3 and described in col. 4, lines 4-14.

13. With respect to claim 6, Mathews teaches the cache memory of claim 5, wherein said source virtual address comprises an address of a virtual memory page, in fig. 3 and described in col. 4, lines 4-14.

14. With respect to claim 8, Mathews teaches the cache memory of claim 1, wherein said load instruction comprises an instruction that explicitly specifies said source virtual address, in fig. 3.

15. With respect to claim 15, Mathews teaches the cache memory of claim 1, further comprising:

a plurality of comparators, coupled to said plurality of storage elements, for comparing said source physical address with a plurality of physical cache line addresses stored in said plurality of storage elements, in col. 3, lines 59-67.

16. With respect to claim 16, Mathews teaches the cache memory of claim 15, further comprising:

a second output, coupled to said plurality of comparators, for indicating said data requested by said load instruction is non speculatively present in the cache memory if said comparator indicates said source virtual address does not match said cache line virtual address does not match said cache line virtual address stored in said top storage element, and said plurality of comparators indicates said source physical address matches one of said plurality of physical cache line addresses stored in said plurality of storage elements, in fig. 5, data line 162. As can be interpreted from the rest of the specification, when the virtual address misses, it retries with the physical address and then the data is output on line 162, indicating a hit.

17. With respect to claim 17, Mathews teaches the cache memory of claim 16, wherein said second output indicates said data requested by said load instruction is non-speculatively present in the cache memory in a second clock cycle subsequent to a first clock cycle in which said output indicates said data requested by said load instruction is not present in the cache memory, in the Abstract.

18. With respect to claim 18, Mathews teaches the cache memory of claim 1, wherein a computer data signal embodied in a transmission medium comprising computer-readable program code provides the cache memory, in fig. 5, control logic 170.

19. With respect to claim 19, Mathews teaches the cache memory of claim 1, a computer program product comprising a computer usable medium having computer readable program code causes the cache memory, wherein said computer program product is for use with a computing device, in fig. 5, control logic 170.

20. With respect to claim 20, Mathews teaches a microprocessor, comprising:

a first cache memory, for caching data specified by push instructions, said first cache memory comprising a last-in-first-out (LIFO) stack memory having a top entry for storing a cache line of data associated with newest push instruction data, in fig. 1 and fig. 5, processor 10 and cache 12. In one embodiment of Mathews invention, this memory can act as a LIFO. See col. 5, lines 20-27, where it is disclosed that stack push and pop operations can be performed. It is also apparent from the specification that this memory array stores both a virtual address and physical address, as the memory array can be accessed by both virtual and physical address;

a second cache memory for caching data specified by non-push memory access instructions, said second cache memory comprising a non-LIFO memory, in fig. 1, external cache 20; and

control logic, coupled to said first and second cache memories, for causing said first cache memory to speculatively provide from said top entry data specified by a load instruction, if a virtual address specified by said load instruction matches a virtual address of said cache line stored in said top entry, in col. 5, lines 28-36.

21. With respect to claim 21, Mathews teaches the microprocessor of claim 20, wherein if said virtual address does not match said virtual address of said cache line stored in said top entry, but if a physical address translated from said virtual address specified by said load instruction matches a physical address of one of a plurality of cache lines stored in said first cache memory, then said control logic causes said first

cache memory to non-speculatively provide said data specified by said load instruction from said matching one of said plurality of cache lines, in col. 5, lines 28-36.

22. With respect to claim 23, Mathews teaches the microprocessor of claim 20, further comprising:

a plurality of physical address comparators, coupled to said control logic, for detecting a condition in which said control logic incorrectly caused said first cache memory to speculatively provide from said top entry data specified by said load instruction, in fig. 5, comparators 130 and 140.

23. With respect to claim 26, Mathews teaches the microprocessor of claim 20, wherein said control logic causes said first cache memory to speculatively provide from said top entry said data specified by said load instruction if said virtual address specified by said load instruction matches said virtual address of said cache line stored in said top entry, prior to determining whether a physical address translated from said virtual address specified by said load instruction matches a physical address of said cache line stored in said top entry, in col. 2, lines 35-43.

24. With respect to claim 27, Mathews teaches a method for performing a speculative load operation from a stack memory cache, the method comprising:

storing stack memory data into a cache memory in a last-in-first-out (LIFO) manner, in col. 5, lines 20-27;

determining whether a physical address of the load instruction matches a physical address of the data stored in the top entry, in col. 5, lines 34-36; and

providing the data from the top entry if the virtual address of the load instruction matches the virtual address of the data stored in the top entry, but before said determining whether the physical address of the load instruction matches the physical address of the data stored in the top entry, in col. 2, lines 35-43.

25. With respect to claim 28, Mathews teaches the method of claim 27, further comprising:

translating the physical address of the load instruction from the virtual address of the load instruction, prior to said determining whether the physical address of the load instruction matches the physical address of the data stored in the top entry, in col.2, lines 35-43.

26. With respect to claim 29, Mathews teaches the method of claim 28, wherein said translating the physical address of the load instruction from the virtual address of the load instruction is performed substantially in parallel with said determining whether the virtual address of the load instruction matches the virtual address of data stored in the top entry of the cache memory, in col. 4, lines 45-51. Referring to fig. 5, the virtual address 100 is supplied to both the TLB 110 for virtual to physical address translation and to the MUX 120 for accessing the memory array 160 at the same time.

27. With respect to claim 30, Mathews teaches the method of claim 28, wherein said translating the physical address of the load instruction from the virtual address of the load instruction is performed by a translation lookaside buffer, in col. 3, lines 61-63.

28. With respect to claim 31, Mathews teaches the method of claim 28, wherein said translating the physical address of the load instruction from the virtual address of the

load instruction comprises translating a virtual memory page address to a physical memory page address, in col. 4, lines 4-14.

29. With respect to claim 32, Mathews teaches the method of claim 27, further comprising:

generating an exception signal, after said providing the data from the top entry if the virtual address of the load instruction matches the virtual address of the data stored in the top entry, if the physical address of the load instruction does not match the physical address of the data stored in the top entry, in fig. 5, prediction wrong signal 178.

30. With respect to claim 33, Mathews teaches the method of claim 32, wherein the exception signal indicates the data provided to the load instruction from the top entry was incorrect data, in col. 5, lines 29-36.

31. With respect to claim 34, Mathews teaches the method of claim 32, further comprising:

providing correct data to the load instruction in response to said exception signal, in col. 5, lines 34-36.

32. With respect to claim 35, Mathews teaches the method of claim 34, wherein said providing correct data to the load instruction in response to said exception signal comprises a microprocessor comprising the cache memory executing a microcode routine to provide the correct data, in fig. 5, processor 10 and control logic 170.

33. With respect to claim 38, Mathews teaches a computer data signal embodied in a transmission medium, comprising:

computer-readable program code for providing a cache memory, said program code comprising:

first program code for providing a plurality of storage elements, arranged as a last-in-first-out memory, having a top one of said plurality of storage elements for storing a cache line of data specified by a plurality of most-recent push instructions, and for storing a virtual address and a physical address of said cache line, in fig. 5, memory array 160. In one embodiment of Mathews invention, this memory can act as a LIFO. See col. 5, lines 20-27, where it is disclosed that stack push and pop operations can be performed. It is also apparent from the specification that this memory array stores both a virtual address and physical address, as the memory array can be accessed by both virtual and physical address;

second program code for providing a comparator, coupled to said top storage element, for comparing said cache line virtual address with a source virtual address of data requested by a load instruction, in fig. 5, comparator 140 and described in col. 5, lines 28-30; and

third program code for providing an output, coupled to said comparator, for indicating said data requested by said load instruction is present in the cache memory if said comparator indicates said source virtual address matches said cache line virtual address stored in said top storage element, prior to determining whether a source physical address of said data requested by said load

instruction matches said physical cache line address, in fig. 5, prediction wrong signal 178. See the related discussion in col. 5, lines 28-36.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

36. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mathews as applied to claims 1-6, 8, 15-21, 23, 26-35 and 38 above, in view of Krolak et al., US Patent 5,751,990.

37. Mathews teaches all other limitations of the parent claims as discussed supra, but fails to teach that the address can be hashed. Krolak et al. resolves this deficiency in col. 5, lines 13-15. Krolak et al. hashes the physical address. Therefore the combination of Mathews and Krolak et al. teach:

The cache memory of claim 2, wherein said source virtual address and said virtual cache line address comprise said untranslated lower portion of said source physical address and said physical cache line address, respectively, wherein said source virtual address and said virtual cache line address each further comprise an upper portion of hashed untranslated address bits appended to said untranslated lower portion.

38. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Krolak et al. before him at the time the invention was made to modify the cache memory system of Mathews with the cache memory system of Krolak et al. in order to improve cache hit rate, as taught by Krolak et al. in col. 5, lines 13-15.

39. Claims 9-14, 22, 24-25 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathews as applied to claims 1-6, 8, 15-21, 23, 26-35 and 38 above, in view of Lynch, US Patent 5,930,820.

40. With respect to claim 9, Matthews teaches all other limitations of the parent claims as discussed supra, but fails to go into sufficient detail to describe a stack pointer. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches:

The cache memory of claim 1, wherein said load instruction comprises an instruction that does not implicitly specify said source virtual address relative to a stack pointer register value, in col. 4, lines 64-67.

41. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order to provide quicker access to the data in the stack, as taught by Lynch in col. 2, lines 32-34.

42. With respect to claim 10, Mathews teaches all other limitations of the parent claims as discussed supra, but fails to go into sufficient detail to describe a stack pointer. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches:

The cache memory of claim 1, wherein each of said push instructions comprises an instruction that implicitly specifies a memory address of said data stored in said cache line relative to a stack pointer register value, in the Abstract, lines 4-6.

43. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order to provide quicker access to the data in the stack, as taught by Lynch in col. 2, lines 32-34.

44. With respect to claim 11, Mathews teaches all other limitations of the parent claims as discusses supra. With reference to fig. 1, of Mathews, it is apparent that when internal cache 12 misses, data is then retrieved from external cache 20 (col. 3, lines 41-46). Although Mathews' invention probably works in the manner described by the present claim, the Examiner believes at this time that Mathews does not describe it

enough detail to anticipate Applicant's claim. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches the cache memory of claim 1, further comprising:

a second comparator, coupled to said plurality of storage elements, for comparing said source physical address with said physical cache line address, in col. 11, lines 24-31.

45. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order to allow access to a second level of cache, thus allowing for both an ideal situation where data is access quickly in a stack (col. 2, lines 31-22 of Lynch) and a next-to-ideal situation where data is accessed by address in a second cache area, before main memory is accessed.

46. With respect to claim 12, Mathews and Lynch teach all other limitations of the parent claims as discussed supra. Lynch further teaches the cache memory of claim 11, further comprising:

a second output, coupled to said second comparator, for indicating said first output incorrectly indicated that said data requested by said load instruction is present in the cache memory, if said second comparator indicates said source physical address does not match said physical cache line address subsequent to said first output indicating said data requested by said load instruction is present in the cache memory, in fig. 3, Data/Hit line 70.

47. With respect to claim 13, Mathews teaches all other limitations of the parent claims as discussed supra, but fails to mention offset to access a next-to-top storage element of the cache. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches the cache memory of claim 1, further comprising:

a second comparator, coupled to said plurality of storage elements, for comparing said source virtual address with a virtual address of a cache line stored in a next-to-top one of said plurality of storage elements, said next-to-top storage element storing a cache line of data specified by a plurality of next-most-recent push instructions to said plurality of most-recent push instructions, in col. 4, lines 41-45. This occurs when the stack pop operation is offset by one.

48. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order to allow access to a second level of cache, thus allowing for both an ideal situation where data is access quickly in a stack (col. 2, lines 31-22 of Lynch) and a next-to-ideal situation where data is accessed by address in a second cache area, before main memory is accessed.

49. With respect to claim 14, Mathews and Lynch teach all other limitations of the parent claims as discussed supra. Lynch further teaches:

The cache memory of claim 13, wherein said first output indicates said data requested by said load instruction is present in the cache memory if said second

comparator indicates said source virtual address matches said cache line virtual address stored in said next-to-top storage element, prior to determining whether said source physical address matches said physical cache line address of said cache line stored in said next-to-top storage element, in the Abstract. This occurs when the stack pop operation is offset by one.

50. With respect to claim 22, Mathews teaches all other limitations of the parent claims as discusses supra. With reference to fig. 1, of Mathews, it is apparent that when internal cache 12 misses, data is then retrieved from external cache 20 (col. 3, lines 41-46). Although Mathews' invention probably works in the manner described by the present claim, the Examiner believes at this time that Mathews does not describe it enough detail to anticipate Applicant's claim. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches:

The microprocessor of claim 21, wherein if said physical address translated from said physical address translated from said virtual address specified by said load instruction does not match said physical address of any of said plurality of cache lines stored in said first cache memory, said control logic causes said second cache memory to non-speculatively provide said data specified by said load instruction if said physical address translated from said virtual address specified by said load instruction matches a physical address of a cache line stored in said second cache memory, in col. 11, lines 8-15.

51. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order to allow access to a second level of cache, thus allowing for both an ideal situation where data is access quickly in a stack (col. 2, lines 31-22 of Lynch) and a next-to-ideal situation where data is accessed by address in a second cache area, before main memory is accessed.

52. With respect to claim 24, Mathews teaches all other limitations of the parent claims as discussed supra. With reference to fig. 1, of Mathews, it is apparent that when internal cache 12 misses, data is then retrieved from external cache 20 (col. 3, lines 41-46). Although Mathews' invention probably works in the manner described by the present claim, the Examiner believes at this time that Mathews does not describe it enough detail to anticipate Applicant's claim. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches:

the microprocessor of claim 23, wherein said condition is detected based on a determination that a physical address translated from said virtual address specified by said load instruction misses in said first cache memory, in col. 11, lines 8-15 and the Abstract.

53. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order

to allow access to a second level of cache, thus allowing for both an ideal situation where data is access quickly in a stack (col. 2, lines 31-22 of Lynch) and a next-to-ideal situation where data is accessed by address in a second cache area, before main memory is accessed.

54. With respect to claim 25, Mathews teaches all other limitations of the parent claims as discussed supra, but fails to expressly disclose a microcode memory. Lynch teaches:

a microcode memory, coupled to said control logic, for storing microcode instructions for recovering from said condition, in fig. 3, Cache Storage and Control 50.

55. With respect to claim 36, Mathews teaches all other limitations of the parent claims as discusses supra. With reference to fig. 1, of Mathews, it is apparent that when internal cache 12 misses, data is then retrieved from external cache 20 (col. 3, lines 41-46). Although Mathews' invention probably works in the manner described by the present claim, the Examiner believes at this time that Mathews does not describe it enough detail to anticipate Applicant's claim. In the same field of endeavor, Lynch also teaches a data cache with a stack memory for storing data separate from a cache line storage. Lynch teaches the method of claim 27, further comprising:

storing non-stack memory data into a second cache memory into locations of the second cache memory based on an address of the non-stack memory data, in col. 3, lines 18-21; and

determining whether the physical address of the load instruction matches a physical address of data stored in the second cache memory, in col. 2, lines 46-48; and

providing the data from the second cache memory if the physical address of the load instruction matches a physical address of data stored in the second cache memory, in col. 2, lines 59-61.

56. It would have been obvious to one of ordinary skill in the art, having the teachings of Mathews and Lynch before him at the time the invention was made, to modify the data cache system of Mathews with the data cache system of Lynch in order to allow access to a second level of cache, thus allowing for both an ideal situation where data is access quickly in a stack (col. 2, lines 31-22 of Lynch) and a next-to-ideal situation where data is accessed by address in a second cache area, before main memory is accessed.

57. With respect to claim 37, Mathews and Lynch teach all other limitations of the parent claims as discussed supra. Lynch further teaches:

The method of claim 36, wherein said determining whether the physical address of the load instruction matches a physical address of data stored in the second cache memory is performed substantially in parallel with said determining whether the physical address of the load instruction matches the physical address of the data stored in the top entry of the LIFO cache memory, in the Abstract.

Conclusion

58. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to

consider these references fully when responding to this action. The documents cited therein teach similar data cache systems.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
March 15, 2006

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100